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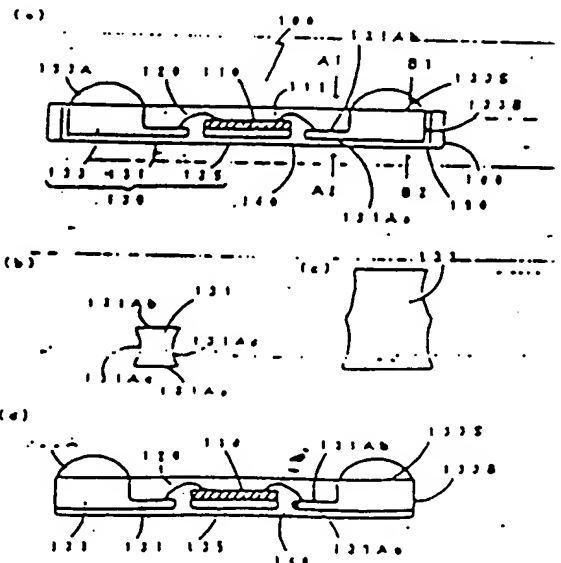
(17)【発明の名称】 紙質封止型平紙体部

(18)【要約】

(19)【発明者】

【目的】 多層化に対応でき、且つ、フタリードの位置ズレや平紙性の向上にも対応できる紙質封止型平紙体部を提供する。

【構成】 一体的に成形したリードフレーム部材と同じ厚さの紙質封止部と積層するための凸状の端子部 133 とを有し、且つ、端子部はインナーリードの片側面にあり、インナーリードに対して厚み方向に突出して設けられており、端子部の先端部に半田等からなる端子部を設け、端子部を封止部から突出させ、端子部の外面側の側面を封止部から突出させており、インナーリードは、断面形状が略円形であり、第 1 面 131 A、第 2 面 131 B、第 3 面 131 C、第 4 面 131 D の 4 面を有しており、かつ第 1 面はリードフレーム部材と同じ厚さの部分の一方の面と同一平面上にあり、第 2 面に向を合っており、第 3 面、第 4 面はインナーリードの内側に向を合っており、凹んだ形状に形成されている。



(4) 研究の目的

(図354) 2段ニッチング加工によりインターリードの厚さがリードフレーム素材の厚さよりも厚みになる構成としたリードフレームを用いたモジュール構成であつて、前記リードフレームは、リードフレーム素材よりも厚みのインターリードと、該インターリードに一時的に固定したリードフレーム素材と同じ厚さの外周部材とを具備するための柱状の端子柱とを有し、且つ、端子柱はインターリードの外周部においてインターリードに対して所定方向に傾斜して設けられており、端子柱の先端部にモジュールからなる端子柱を収め、端子柱を押し戻す際部材から取出させ、端子柱の外周部の外面を押し戻す部材から取出させており、インターリードは、多数段状に該方向で第1段、第2段、第3段、第4面の4面を有しており、かつ第1面はリードフレーム素材と同じ厚さの他の部分の一方の面と同一平面上にあつて第2面に向き合つており、第3面、第4面はインターリードの内側に面かつて凹んだ形状に形成されていることを特徴とする接合防止型モジュール。

(ハス厚2) 2枚ニッティング機によりインターリードの厚さがリードフレームと同等の厚さよりし厚みに外周加工されたリードフレームを用いた本装置を要っており、前述リードフレームは、リードフレームと同等よりし厚みのインターリードと、該インターリードに一時的に装着したリードフレームと異なり該部分の外周面周縁部を形成するための凸状の突起部とを有し、且つ、該突起はインターリードの外周面においてインターリードに対して係合方向に直交して設けられており、該突起の先端の一部を封止用樹脂から露出させて突起部とし、該突起の外周部の側面を封止用樹脂から露出させており、インターリードには、前記基板が18万平方ミリ、第1面、第2面、第3面、第4面の4面を有しており、かつ第1面にリードフレームと異なり該部分の他の部分の一方の面とは一面の上に乗って第2面に向かっており、第3面、第4面はインターリードの内側に向かって凹んだ形状におおわれていることを特徴とする原形封止型半導体装置。

〔読者問〕 第2版にないし？について、第3版電子はインナーリード間にあり、第3版紙体の電磁気はワイヤにてインナーリードと電気的に接続されていることを確認とする理由にどうして第3版は改定。

(注5) リードフレームにおいて、リードフレームにダイパッドを有しており、半導体素子がダイパッド上に搭載され、固定されていることを特徴とする半導体装置。

【2次取り】 2次取りにおいて、リードフレームはダイパッドを傷めないしので、エポキシはインターリードとともに両面固定用テープにより固定されていることを確認とする書写防止型をよば要区。

【図 6】 図 5 のようなしきい値において、ある状態では半導体素子の電圧降下の正をインターリードの第 2 面

に絶縁材料により固定されており、該導体はその
二端はワイヤによりインターリードの溝区と導体
に接続されていることを確認する者は該装置によれば

(図5-7) 日本国にない2において、中央部にはパンクによりインターリードの第2面に固定された状態でインターリードと接続していることを示した。本図は、製品製造工程を示す。

(月 日 年 日)

(0 0 0 1)

（最上との対比図）左列に、主として直線が多量に
に於てと、右列、アフターリードの区画（スニ
ー）やアフターリードの長方形（コブラリチエー）の
のみに於てと、リードフレームを用いた新設計は
を減低させる。

(0 0 0 2)

(反張の防止) 反張より用いられている巻戻防止型のニ
よ体器版 (プラスチックリードフレームパッケージ)

は、一桁に5:5(2)に示されるような組法であり、
ニは番付:5:0をなすダイバッド5:15:10
両者の区別とをなす組法を行うためのアフォーワード
5:15:3。アフォーワード5:15:3に一致となった
インナーワード5:12。5インナーワード5:1
2の先頭部と5:0番付5:15:20の番付5:15:2
とを形式的に区別するためのワイ5:30。本組法

テ1520を対応して外からの応力、内側から与る応力1540からなっており、これはテ1520をリードフレームのダイパッド1511に固定した上に、基板1500により押し立ててパッケージとしたもので、基板1512のダイパッド1521に内側で与る応力のインターリード1513を必要とするものであ

ろ、そして、このような厚肉防止型の半導体素子の成立
 材料として用いられる（主層）リードフレームは、一帯
 には図15（b）に示すような構造のもので、半導体素
 子を固定するためのダイパッド1511と、ダイパッド
 1511の周囲にはけられた半導体素子と導通するための
 インターリード1512、インターリード1512
 に連続して外延形成の金属層を有するもの、スワッチー
 リード1513、厚肉防止層の材料となるダムバー15

14. リードフレーム1510全体を支持するフレーム
(E) 型1515を備えており、通気、カバー、4

28金(4.2×ニッケル-6合金)。刃部は金のような
硬度に育った合金を用い、プレス造りもしくはエッチン
グ法により形成されていた。図 15 (b) (c)
に、図 15 (b) (d) に示すリットフレーム系至四の
F1-F4 3つに相当する断面である。

〔000〕このようなリードフレームを構築した装置
 1. 止留部を形成する（プラスチックリードフレームパッ
 ケージ）において、金属部品の風化防止の手段とし
 て、金属部品の表面処理を行い、小型化かつ高品質の

で、テーピングの工程や、リードフレームを固定するクランプ工程で、ベタははんだを均等に塗くようになった部分との差が顕著になる場合があるので、エッチングを行うエリアはインターリード孔の周辺に限定だけにせず大めにとらねばならない。温度57°C、圧力4.8ボームの酸化第二銅溶液を用いて、スプレーで2.5k Ω /cm²にて、レジストパターンが形成されたリードフレーム素材1110の両面をエッチングし、ベタ（半田）に塗布された第2の3層に塗布した銅でエッチングを止めた。（図11（b））

上記第1回目のエッチングにおいては、リードフレームは1110の状態から同時にエッチングを行ったが、必ずしも基板から同時にエッチングする必要はない。本実施例のように、第1回目のエッチングにおいてリードフレームは1110の状態から同時にエッチングする理由は、基板からエッチングすることにより、仮設する第2回目のエッチング時間を短縮するため、レジストパターン920B減のみの再度エッチングの場合と比べ、第1回目エッチングと第2回目エッチングのトータル時間が短縮される。言い、第一の減成1110の状態とした第一の凹部150Uにエッチングを施し1180としての第2エッチングのあるポットメルト型

MR-WB6) を、ダイオードを剥いて、ニホし、ベタ
板(平塩板)にニホせられた導線の間に1550に詰め込
んだ。レジストパターン1120A上にも同ニッティングを
行った。1180にニホせられた板板とした。(図11
(c))

エッティングを以て1180を、レジストパターン112
— 0Aと全通に配布するを望まないが、一時的に115
0を並び一版にのみ配布することにしよう。

(c) に示すように、第一の凹部 1150 とともに、第一の開口部 1130 が全面にエッチング形成され、1180 を形成した、基板内部で形成したニッチング層 1180 は、アルカリ抵抗層のフックスであるが、基本的にエッチング液に耐性があり、ニッチング時にある程度の耐酸性のあるものが、好ましく、特に、上記フックスに規定された、UV 硬化型のものを用いる。このようにエッチング形成後、1180 をインナーリード形成用の抵抗を形成するためのパターンが形成された基板上の第一の凹部 1150 の内部に埋め込むことにより、後述のニッチング時に第一の凹部 1150 が露出されてスベくならないようにしていることと、同時に、基板端部ニッチング加工に対しての耐腐食性強度を有しており、スプレー性を示す (2.5 kg/cm^2 以上) とすることができ、これによりニッチングが容易に進行しやすくなる。この後、第二凹部のニッチングを所定寸法に（工程図）に露出された第二の凹部 1160 を抵抗層からリードフレーム部 1110 をエッチングし、完成させ、

インターワード証券の代表取締役社長。 (S:)

ス10回のエッチング加工にて作製された、リードフレーム面に所定のエッチング抵抗面に形成されているが、この面を厚み2層はインナーリード側へ向いた面である。ないで、例へ、エッチング抵抗厚9.80のレジスト厚（レジストパターン1120A、1120B）の面を厚み、インナーリード側向131Aが2層に形成された図9（a）に示すリードフレーム120Aを4層、エッチング抵抗厚1.80のレジスト厚（レジストパターン1120A、11280）の面を厚み形成されたリードフレーム面により形成された。

0014) 上に、図1に示すリードフレームの加工工程は、エッチング処理される。インターリードまたはリーディング面においたリードフレームのエッチング加工による露出する方式で、特に、図1に示す、インターリード面の第1区1J、1Aを第2区以外の他の部分と同一に、第2区1J、1Aと方向を定めて形成し、且つ、表面1J1AC、第2区1J1ACをインターリードの面に向かって凹んだ状態にするニッチング加工方法である。従って第2区1Jの形状は各々のようにバンプを有する第2区をインターリードの第2区1J1A、1Bに形成し、インターリードと電気的に接続する場合に

第2図1.3.1.AとBのインナーリード側に凹んだ形は、
 成した方がバンプ振動の周の許容区が大きくなる。
 図12に示すニッチング加工方法が知られる。図1
 示すニッチング加工方法には、第1図Bのニッチング
 によって、図11に示す方法と異じてあろうが、エッチ
 深さは1180と第2図の凹み1160の間にほぼ等
 しい。第1図の凹み1150側から第2図Bのニッチン
 ング、またはエッチングによって、図11に示す第1図B
 ニッチングにて、第2図凹み1140からのニッチン
 ングに当たっており、図12に示すニッチング加工方
 法で得られたリードフレイムのインナーリード長
 度では、図6(b)に示すように、第2図3.3
 がインナーリード側にへこんだ凹みになる。

1.5) m、上記図11、図12に示すエッチング
法のように、エッチングを2段階にわけて行うエ
ッチ加工方法、一般には2段エッチング加工方法
であり、本発明に有利な加工方法である。右図
の図9(a)に示す、リードフレーム130A
においては、3段エッチング加工で、図9(b)
に示すことにより部分的にリードフレーム
を削りながら形成加工をする方法とが提供されて
いる。リードフレームを削り出した部分において
、2段目の加工がどのようにして行われるか、図1
2に示す。上記の方法においては、インターリ
ット1314の形成加工は、右の図9116
と、最終的には互いにインターリット形成部の
位置を一致するので、例えば、図9116を50 μ m

の両方に平等ではあるが、この部分の両者は同様の
ペースをとらない。また両面ともリードフリースペース
である。両面（ボンディング）両面に両面（ボン
ディング）を両面より作る。図1（二）にプレス（ボン
ディング）によりインナーリード元端部を両面化した後に
両面（ボンディング）によりインナーリード元端部（100：0
100）100を加えたものの、両面（ボンディング）（図示す
との両面（ボンディング）を示したものであるが、こ
れはプレス（ボンディング）が両面に両面（ボンディング）
の、どちらの面を用いて両面（ボンディング）して
b、図1（二）の（a）、（b）に示すように両面
（ボンディング）の面に両面（ボンディング）が両面（ボン
ディング）が多い。a、100：100（a）は両面（ボン
ディング）

[illegible]

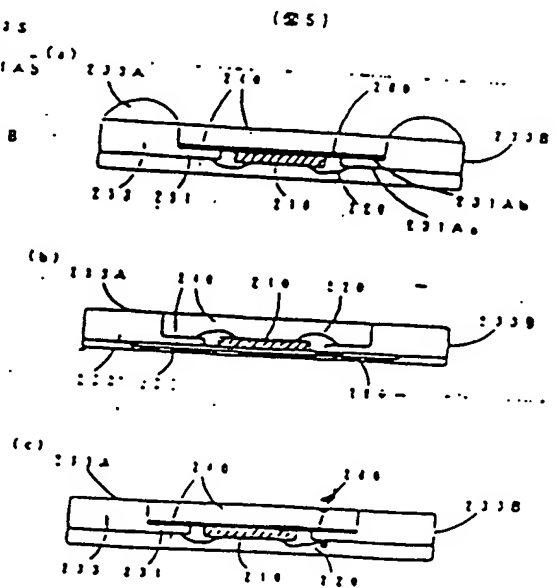
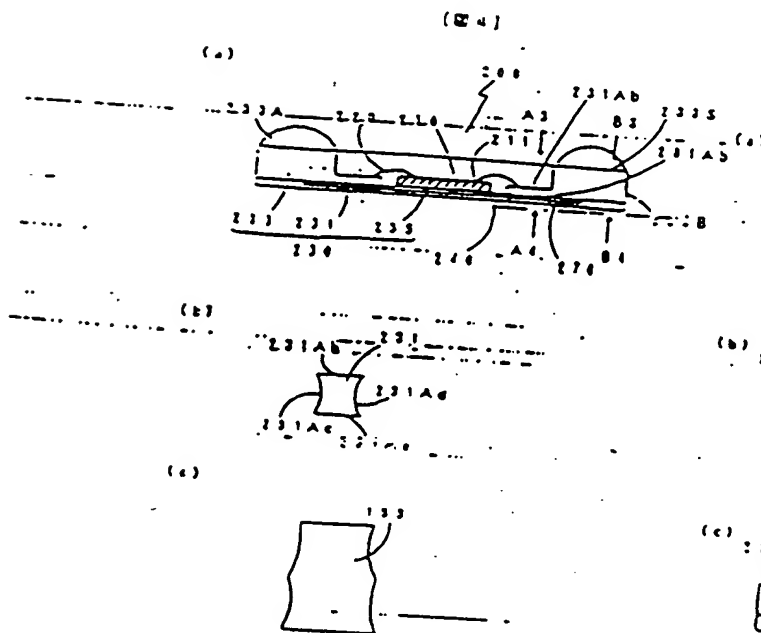
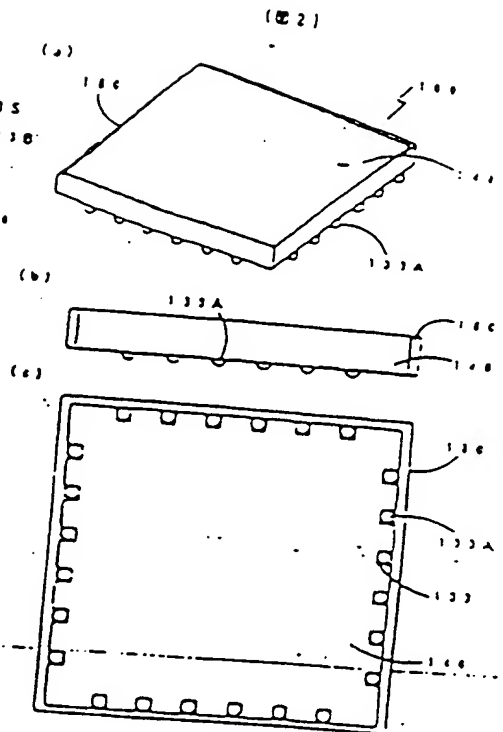
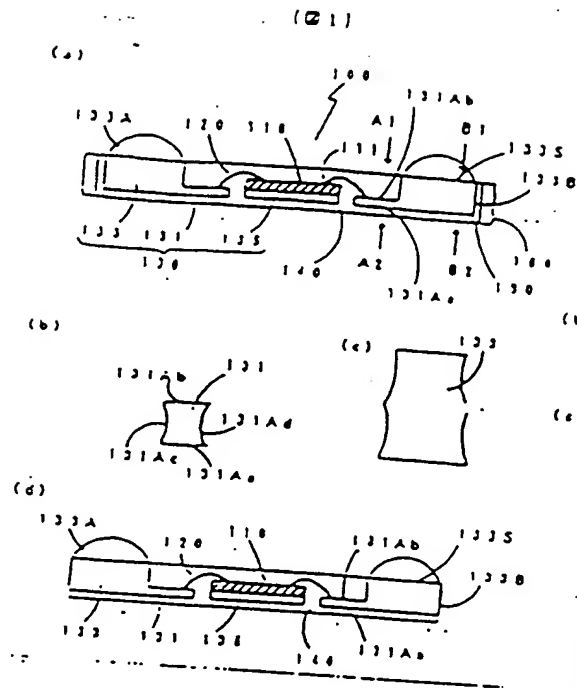
もで、ダイパッド図1305が外空に存在している。ダイ
パッド図1305が外空に存在していることにより、天
板例1)に比べ、熱の伝わり性が低れている。図3(b)に
示す変形例の構造は各層より、ダイパッド図1305が外空
に存在させているものであり、天板例1)に比べ、熱の伝
わり性が低れている。変形例1や図3(a)に示す変形例
とは、導体は電子110の向と角があるため、ワイヤボン
ディング面をリードフレームの裏面に設けている。図3
(c)(d)図3(d)、図3(c)に示す変形例には、それぞれ
変形例1、図3(a)に示す変形例、図3(b)に
示す変形例において、導体の電圧からなる導体を反
映せず、電子伝導面を底層基板として用いているので
あり、製造工程を単純化した構造となっている。

(0019) 本発明の実施形態の一例として、導体は電子
を導く。図4(a)に実施形態の導体構造を示す。導体は二
重の断面図であり、図4(b)に導体のA-A'線
におけるインターリード部の断面図で、図4(c)は
図4(a)のB-B'線における導体部の断面図であ
る。即ち、実施形態の導体は底層の外側に実施例1と同じ
構造となる導体部を有する。図4中、2700は導体部
である。2710は導体部、2711は導体部(パッ
ド)。2720はワイヤ、2730はリードフレーム、27
40はインターリード部、2750はA-A'線、2760はB-
B'線、2770はC-C'線、2780はD-D'線、2790はE-E'
線、2791はF-F'線、2792はG-G'線、2793はH-H'
線、2794はI-I'線、2795はJ-J'線、2796はK-K'
線、2797はL-L'線、2798はM-M'線、2799はN-N'
線、2799AはO-O'線、2799BはP-P'線、2799CはQ-Q'
線、2799DはR-R'線、2799EはS-S'線、2799FはT-T'
線、2799GはU-U'線、2799HはV-V'線、2799IはW-W'
線、2799JはX-X'線、2799KはY-Y'線、2799LはZ-Z'
線、2799MはAA'-AA'線、2799NはBB'-BB'線、2799OはCC'-CC'
線、2799PはDD'-DD'線、2799QはEE'-EE'線、2799RはFF'-FF'
線、2799SはGG'-GG'線、2799TはHH'-HH'線、2799UはII'-II'
線、2799VはJJ'-JJ'線、2799WはKK'-KK'線、2799XはLL'-LL'
線、2799YはMM'-MM'線、2799ZはNN'-NN'線、2799AAはOO'-OO'
線、2799ABはPP'-PP'線、2799ACはQQ'-QQ'線、2799ADはRR'-RR'
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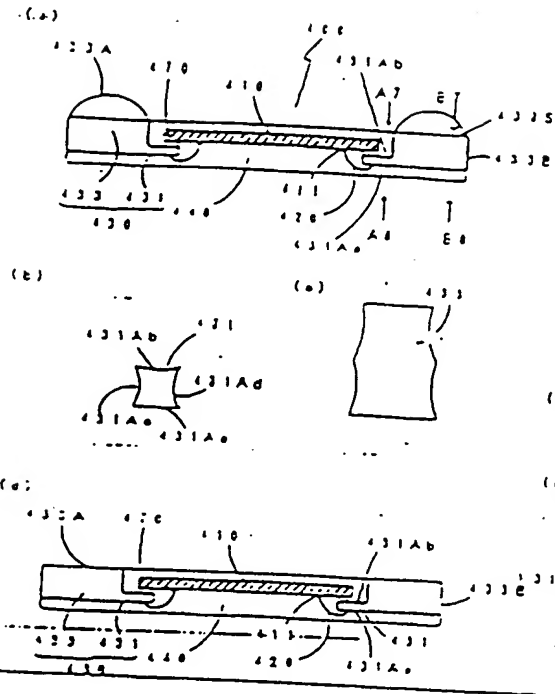
(1025) はいて、第4図の原理防止型を第22
を要する。第7(a)に第4図の原理防止型を第22
の断面図であり、第7(b)に第7(a)のA7-A
8におけるインターリード部の断面図で、第6(c)に
第6(a)の第7-98における第22部の断面図であ
る。第4図の原理防止型の第22部は第4図1とは
同じとなる。図は省略した。第7中、500には第
22部、410には第22部、411にはバンド、430に

190
 260
 270
 350
 470
 1110
 1120A, 1120B
 1130
 1140
 1150
 1160
 1170
 1180
 1320B, 1320C, 1320D
 1321B, 1321C, 1321D
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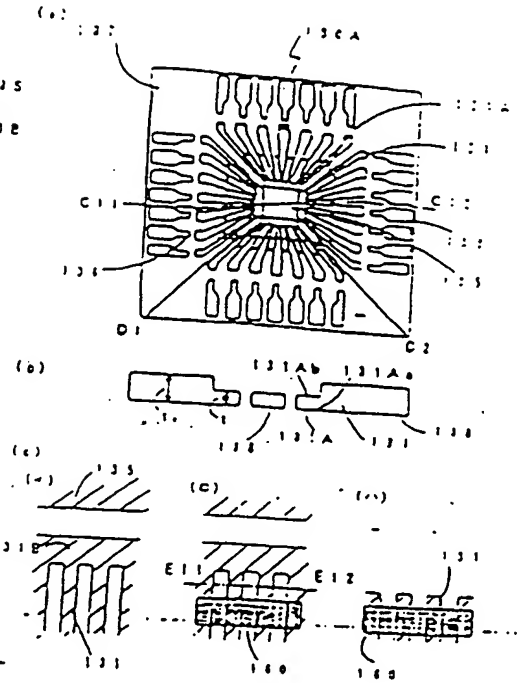
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 1331A
 イニング面
 1410
 ードフレイムニ面
 1420
 オトレジスト
 1430
 ジストパターン
 1440
 シターリード
 1510
 ードフレイム
 1511
 イパッド
 1512
 シターリード
 1512A
 シターリード先頭部
 1513
 フターリード
 1514
 ムバー
 1515
 レーム部 (内部)
 1520
 部品表示
 1521
 部品 (パッド)
 1530
 1540
 止角部



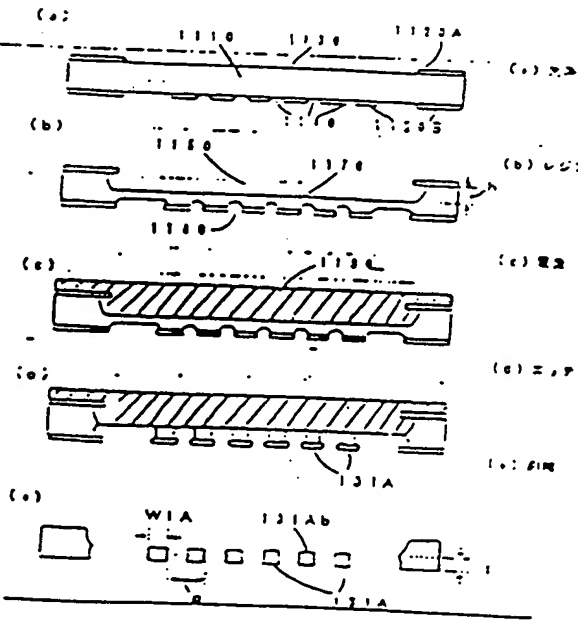
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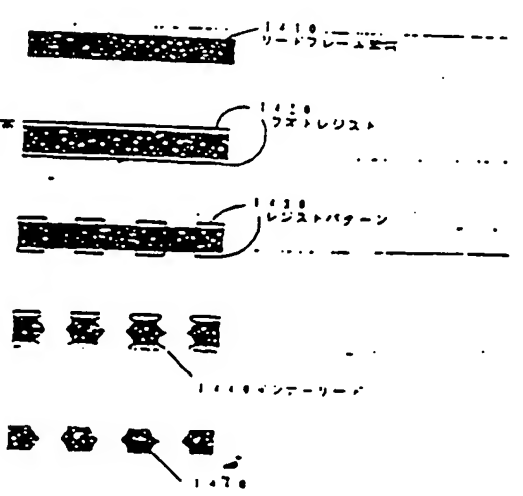
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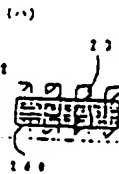
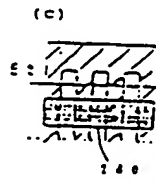
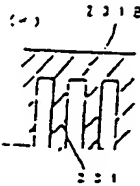
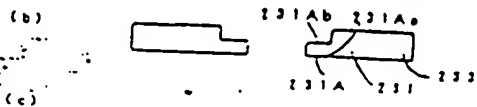
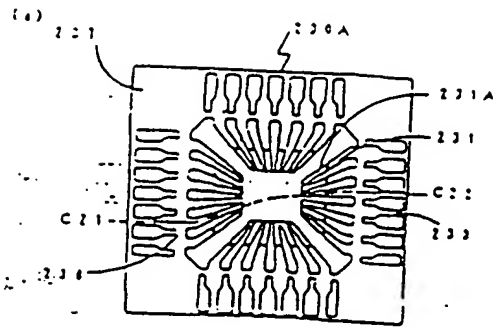
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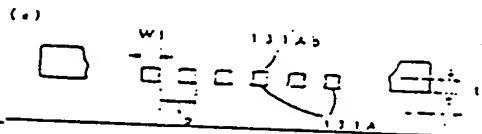
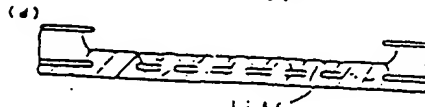
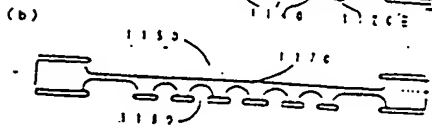
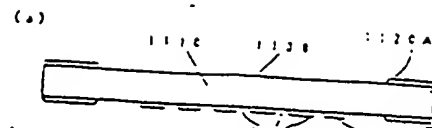
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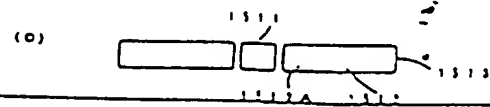
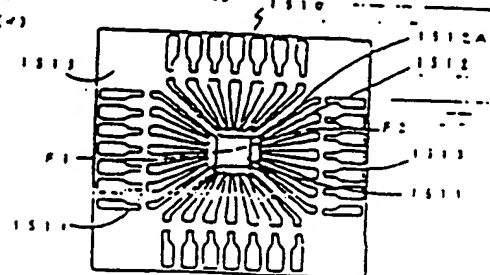
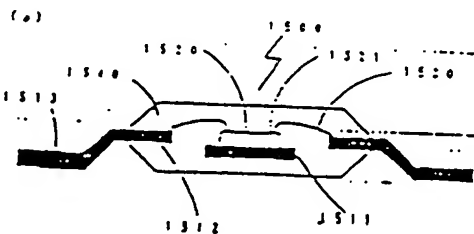
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Japanese Patent Laid-Open Publication No. Heisei 9-8205

[TITLE OF THE INVENTION]

RESIN-ENCAPSULATED SEMICONDUCTOR DEVICE

5

[CLAIMS]

1. A resin-encapsulated semiconductor device using
a lead frame which is shaped in accordance with a two-step
etching process to a body wherein a thickness of inner
10 leads is less than that of the lead frame blank,
comprising:

inner leads having the thickness less than that of the
lead frame blank; and

15 terminal columns integrally connected to the inner
leads and having the same thickness with the lead frame
blank, the terminal columns possessing a column-shaped
configuration which is adapted to be electrically connected
to an external circuit, the terminal columns being disposed
outside of the inner leads in a manner such that they are
20 coupled to the inner leads in a direction orthogonal to the
thickness-wise direction thereof, the terminal columns
having terminal portions arranged on top ends thereof, the
terminal portions being made of solders, etc. and exposed
to the outside beyond a resin encapsulate, each inner lead
25 possessing a rectangular cross-section and having four

surfaces including a first surface, a second surface, a
third surface and a fourth surface, the first surface being
flushed with one surface of a remaining portion of the
inner lead having the same thickness with the lead frame
blank while being opposed to the second surface, and each
5 of the third and fourth surfaces having a concave shape
depressed toward the inside of the inner lead.

2. A resin-encapsulated semiconductor device using
10 a lead frame which is shaped in accordance with a two-step
etching process to a body wherein a thickness of inner
leads is less than that of the lead frame blank,
comprising:

inner leads having the thickness less than that of the
15 lead frame blank; and

terminal columns integrally connected to the inner
leads and having the same thickness with the lead frame
blank, the terminal columns possessing a column-shaped
configuration which is adapted to be electrically connected
20 to an external circuit, the terminal columns being disposed
outside of the inner leads in a manner such that they are
coupled to the inner leads in a direction orthogonal to the
thickness-wise direction thereof, portions of top ends of
the terminal columns being exposed to the outside beyond a
25 resin encapsulate, each inner lead possessing a rectangular

cross-section and having four surfaces including a first surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the inside of the inner lead.

3. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein a semiconductor chip is received inward of the inner leads, and electrodes of the semiconductor chip are electrically connected to the inner leads through wires, respectively.

4. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame has a die pad, and the semiconductor chip is mounted onto the die pad.

5. The resin-encapsulated semiconductor device as claimed in claim 3, wherein the lead frame does not have a die pad, and the semiconductor chip is fastened to the inner leads using a reinforcing fastener tape.

6. The resin-encapsulated semiconductor device as

claimed in claims 1 or 2, wherein the semiconductor chip is fastened by means of insulating adhesive to the second surfaces of the inner leads on one surface thereof on which the electrodes are located, and the electrodes of the semiconductor chip are electrically connected to the first surfaces of the inner leads through wires, respectively.

7. The resin-encapsulated semiconductor device as claimed in claims 1 or 2, wherein the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads.

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF THE INVENTION]

The present invention relates to a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals and resolving problems which are caused in association with position shift and coplanarity of an outer lead.

[DESCRIPTION OF THE PRIOR ART]

FIG. 15(a) shows the configuration of a generally known resin-encapsulated semiconductor device (a plastic lead frame package). The shown resin-encapsulated semiconductor device includes a die pad 1511 having a

semiconductor chip 1520 mounted thereon, outer leads 1513
to be electrically connected to the associated circuits,
inner leads 1512 formed integrally with the outer leads
1513, bonding wires 1530 for electrically connecting the
5 tips of the inner leads 1512 to the bonding pad 1521 of the
semiconductor chip 1520, and a resin 1540 encapsulating the
semiconductor chip 1520 to protect the semiconductor chip
1520 from external stresses and contaminants. This resin-
encapsulated semiconductor device, after mounting the
10 semiconductor chip 1520 on the bonding pad 1521, is
manufactured by encapsulating the semiconductor chip 1520
with the resin. In this resin-encapsulated semiconductor
device, the number of the inner leads 1512 is equal to that
of the bonding pads 1521 of the semiconductor chip 1520.
15 And, FIG. 15(b) shows the configuration of a monolayer lead
frame used as an assembly member of the resin-encapsulated
semiconductor device shown in FIG. 15a. Such a lead frame
includes the bonding pad 1511 for mounting the
semiconductor chip, the inner leads 1512 to be electrically
20 connected to the semiconductor chip, the outer lead 1513
which is integral with the inner leads 1512 and is to be
electrically connected to the associated circuits. This
also includes dam bars 1514 serving as a dam when
encapsulating the semiconductor chip with the resin, and a
25 frame 1515 serving to support the entire lead frame 1510.

Such a lead frame is formed from a highly conductive metal such as a cobalt, 42 alloy (a 42% Ni-Fe alloy), copper-based alloy by a pressing working process or an etching process. FIG. 15(b)(D) is a cross-sectional view taken along the line F1-F2 of FIG. 15(b)(1).

Recently, there has been growing demand for the miniaturization and reduction in thickness of resin-encapsulated semiconductor device employing lead frames like the lead frame (plastic lead frame package) and the increase of the number of terminals of resin-encapsulated semiconductor package as electronic apparatuses are miniaturized progressively and the degree of the integration of semiconductor device increase progressively. Thus, recent resin-encapsulated semiconductor package, particularly quad plate package (QFPs) and thin quad flat packages (TQFPs) have each a greatly increased number of pins.

Lead frames having inner leads arranged at small pitches among lead frames for semiconductor packages are fabricated by a photolithographic etching process, while lead frames having inner leads arranged at comparatively large pitches among lead frames for semiconductor packages are fabricated by press working. However, lead frames having a large number of fine inner leads to be used for forming semiconductor packages having a large number of

Pins are fabricated by subjecting a blank of a thickness on the order of 0.25 mm to an etching process, not a press working.

5 The etching process for forming a lead frame having fine inner leads will be described hereinafter with reference to FIG. 14. First, a copper alloy or 42 alloy thin sheet of a thickness on the order of 0.25 mm (a lead frame blank 1410) is cleaned perfectly (FIG. 14(a)). Then, a photoresist, such as a water-soluble casein photoresist containing potassium dichromate as a sensitive agent, is spread in photoresist films 1420 over the major surfaces of the thin film as shown in FIG. 14(b).

10 Then, the photoresist films are exposed, through a mask of a predetermined pattern, to light emitted by a high-pressure mercury lamp, and the thin sheet is immersed in a developer for development to form a patterned photoresist film 1430 as shown in FIG. 14(c). Then, the thin sheet is subjected, when need be, to a hardening process, a washing process and such, and then an etchant containing ferric chloride as a principal component is sprayed against the thin sheet 1410 to etch through portions of the thin sheet 1410 not coated with the patterned photoresist films 1420 so that inner leads of predetermined sizes and shapes are formed as shown in FIG. 14(d).

15
20
25

Then, the patterned resist films are removed, the patterned thin sheet 1410 is washed to complete a lead frame having the inner leads of desired shapes as shown in FIG. 14(e). Predetermined areas of the lead frame thus formed by the etching process are silver-plated. After being washed and dried, an adhesive polyimide tape is stuck to the inner leads for fixation, predetermined tab bars are bent, when need be, and the die pad depressed. In the etching process, the etchant etches the thin sheet in both the direction of the thickness and directions perpendicular to the thickness, which limits the miniaturization of inner lead pitches of lead frames. Since the thin sheet is etched from both the major surfaces as shown in FIG. 14 during the etching process, it is said, when the lead frame has a line-and-space shape, that the smallest possible intervals between the lines are in the range of 50 to 100% of the thickness of the thin sheet. From the viewpoint of forming the outer lead having a sufficient strength, generally, the thickness of the thin sheet must be about 0.125 mm or above. Furthermore, the width of the inner leads must be in the range of 70 to 80 μ m for successful wire bonding. When the etching process as illustrated in FIG. 14 is employed in fabricating a lead frame, a thin sheet of a small thickness in the range of 0.125 to 0.15 mm is used and inner leads are formed by etching so that the

fine tips thereof are arranged at a pitch of about 0.1 mm.

However, recent miniature resin-encapsulated semiconductor package requires inner leads arranged
5 pitches in the range of 0.13 to 0.15 mm, far smaller than 0.163 mm. When a lead frame is fabricated by processing thin sheet of a reduced thickness, the strength of the outer leads of such a lead frame is not large enough to withstand external forces that may be applied thereto in the subsequent processes including an assembling process and a chip mounting process. Accordingly, there is a limit to the reduction of the thickness of the thin sheet to enable the fabrication of a minute lead frame having fine leads arranged at very small pitches by etching.

15 An etching method previously proposed to overcome such difficulties subjects a thin sheet to an etching process to form a lead frame after reducing the thickness of portions of the thin sheet corresponding to the inner leads of the lead frame by half etching or pressing to form
20 the fine inner leads by etching without reducing the strength of the outer leads. However, problems arise in accuracy in the subsequent processes when the lead frame is formed by etching after reducing the thickness of the portions corresponding to the inner leads by pressing; for
25 example, the smoothness of the surface of the plated areas

is unsatisfactory, the inner leads cannot be formed in a flatness and a dimensional accuracy required to clamp the lead frame accurately for bonding and molding, and a platemaking process must be repeated twice making the lead fabricating process intricate. It is also necessary to repeat a platemaking process twice when the thickness of the portions of the thin sheet corresponding to the inner leads is reduced by half etching before subjecting the thin sheet to an etching process for forming the lead frame, which also makes the lead frame fabricating process intricate. Thus, this previously proposed etching method has not yet been applied to practical lead frame fabricating processes.

(SUBJECT MATTERS TO BE SOLVED BY THE INVENTION)

On the other hand, because a pitch among inner leads is made narrow as the number of terminals is increased, it is considered important to know whether a problem is caused or not in association with position shift or coplanarity of an outer lead when implementing a chip mounting process. Accordingly, the present invention has been made in an effort to solve the problems occurring in the related art, and an object of the present invention is to provide a resin-encapsulated semiconductor device capable of meeting the requirement for an increase in the number of terminals

and resolving problems which are caused in association with position shift and coplanarity of an outer lead.

[MEANS FOR SOLVING THE SUBJECT MATTERS]

5 According to one aspect of the present invention, there is provided a resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank, comprising: inner leads having the thickness less than
10 of the lead frame blank; and terminal columns electrically connected to the inner leads and having the same thickness as with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the
15 columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, the terminal columns having terminal portions
20 arranged on top ends thereof, the terminal portions being made of solders, etc. and exposed to the outside beyond the resin encapsulate, outer surfaces of the terminal columns also being exposed to the outside beyond the resin encapsulate, each inner lead possessing a rectangular
25 cross-section and having four surfaces including a

surface, a second surface, a third surface and a fourth surface, the first surface being flushed with one surface of a remaining portion of the inner lead having the same thickness with the lead frame blank while being opposed to the second surface, and each of the third and fourth surfaces having a concave shape depressed toward the first surface of the inner lead.

According to another aspect of the present invention there is provided a resin-encapsulated semiconductor device using a lead frame which is shaped in accordance with a two-step etching process to a body wherein a thickness of inner leads is less than that of the lead frame blank comprising: inner leads having the thickness less than that of the lead frame blank; and terminal columns integrally connected to the inner leads and having the same thickness with the lead frame blank, the terminal columns possessing a column-shaped configuration which is adapted to be electrically connected to an external circuit, the terminal columns being disposed outside of the inner leads in a manner such that they are coupled to the inner leads in a direction orthogonal to the thickness-wise direction thereof, portions of top ends of the terminal columns being exposed to the outside beyond a resin encapsulate, outer surfaces of the terminal columns also being exposed to the outside beyond the resin encapsulate, each inner lead

possessing a rectangular cross-section and having four
surfaces including a first surface, a second surface, a
third surface and a fourth surface, the first surface being
flushed with one surface of a remaining portion of the
5 inner lead having the same thickness with the lead frame
blank while being opposed to the second surface, and each
of the third and fourth surfaces having a concave shape
depressed toward the inside of the inner lead.

According to another aspect of the present invention,
10 a semiconductor chip is received inward of the inner leads,
and electrodes (pads) of the semiconductor chip are
electrically connected to the inner leads through wires,
respectively. According to another aspect of the present
invention, the lead frame has a die pad, and the
15 semiconductor chip is mounted onto the die pad. According
to another aspect of the present invention, the lead frame
does not have a die pad, and the semiconductor chip is
fastened to the inner leads using a reinforcing fastener
tape. According to still another aspect of the present
20 invention, the semiconductor chip is fastened by means of
insulating adhesive to the second surfaces of the inner
leads on one surface thereof on which the electrodes are
located, and the electrodes of the semiconductor chip are
electrically connected to the first surfaces of the inner
25 leads through wires, respectively. According to yet still

another aspect of the present invention, the semiconductor chip is fastened to the second surfaces of the inner leads by bumps thereby to be electrically connected to the inner leads. In the above descriptions, in the case that the terminal columns have terminal portions which are arranged on top ends of the terminal columns, with the terminal portions made of solders, etc. and exposed to the outside beyond the resin encapsulate, while it is the norm that the terminal portions comprising the solders, etc. are exposed to the outside beyond the resin encapsulate, it is not necessarily required for the terminal portions to be projected beyond the resin encapsulate. Moreover, while it is possible to use the outside surfaces of the terminal columns while they are not encapsulated by the resin encapsulate and they are exposed to the outside, the outside surfaces of the terminal columns which are not encapsulated by the resin encapsulate, can be covered by a protective frame using adhesive, etc.

20 [WORKING FUNCTIONS]

The resin-encapsulated semiconductor device in accordance with the present invention can meet a demand for an increase in the number of terminals. At the same time, in the resin-encapsulated semiconductor device, because the forming process of the outer leads as in the case of using

a mono-layered lead frame shown in FIG. 13(b) is not required, it is possible to provide a semiconductor device in which no problems are caused in association with position shift and coplanarity of the outer leads. More particularly, the use of a multi-pinned lead frame shaped in a manner that inner leads have a thickness less than that of the lead frame blank by a two-step etching process, that is, the inner leads are arranged at a fine pitch, can meet a demand for an increase in the pin number of the semiconductor device. Furthermore, by using the lead frame which is fabricated by a two-step etching process as will be described later with reference to FIG. 1, the second surface of each inner lead has coplanarity, and is excellent in wire-bonding property. In addition, since the first surface of the inner lead is also a flat surface and the third and fourth surfaces are depressed toward the inside of the inner lead, the inner leads are stable and coplanarity width upon wire bonding process can be enlarged.

[EMBODIMENTS]

Embodiments of the resin-encapsulated semiconductor device in accordance with the present invention will now be described with reference to the attached drawings. First, a resin-encapsulated semiconductor device in accordance

With a first embodiment of the present invention described hereinafter with reference to FIGS. 1 and 2, FIG. 1(a) is a cross-sectional view of the encapsulated semiconductor device according to the embodiment of the present invention. FIG. 1(b) is a sectional view of an inner lead taken along the line of FIG. 1(a), and FIG. 1(c) is a cross-sectional view of a terminal column taken along the line B1-B2 of FIG. 1(a). Moreover, FIG. 2(a) is a perspective view of the encapsulated semiconductor device according to the embodiment of the present invention, FIG. 2(b) is a top view of the resin-encapsulated semiconductor device of FIG. 2(a), and FIG. 2(c) is a bottom view of the encapsulated semiconductor device of FIG. 2(a). In FIGS. 1 and 2, a drawing reference numeral 100 represents an encapsulated semiconductor device, 110 a semiconductor chip, 111 electrodes (pads), 120 wires, 130 a lead frame, 131 inner leads, 131Aa a first surface, 131Ab a second surface, 131Ac a third surface, 131Ad a fourth surface, 132A terminal columns, 133A terminal portions, 133B side surfaces, 133S a top surface, 135 a die pad, and 140 a resin encapsulate.

In the resin-encapsulated semiconductor device according to the first embodiment, as shown in FIG. 1, the semiconductor chip 110 is placed inward of the

leads 131. As can be readily seen from FIG. 1(a), the semiconductor chip 110 is mounted on the die pad 131 at the surface thereof which is opposed to the other surface thereof where the electrodes pads 111 of the semiconductor chip 110 are arranged. Each electrode pad 111 is electrically connected to the second surface 131a of the inner lead 131 through the wire 120. The electrical connection between the resin-encapsulated semiconductor device 100 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 100 via the terminal portions 133a each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 133a located on the top surfaces 133 of the terminal columns 133, respectively. In the resin-encapsulated semiconductor device of the first embodiment of the present invention, it is not necessarily required to provide a protective frame 190, and instead, a structure, as shown in FIG. 1(d), in which no protective frame is used can be adopted.

The lead frame 130 used in the semiconductor device 100 according to the first embodiment is made of a 42% nickel-iron alloy. Therefore, the lead frame 130A which has a contour as shown in FIG. 9(a) and is shaped by an etching process, is used as the lead frame 130. The lead frame 130 has inner leads 131 which are shaped to have a

thickness less than that of the terminal columns 133 or other portions. Dam bars 136 serve as a dam when encapsulating the semiconductor chip 110 with a resin. Moreover, although the lead frame 130A which is processed by etching to have the contour as shown in FIG. 9A is used in this embodiment, the lead frame is not limited to such a contour because portions except the inner leads 131 and the terminal columns 133 are not necessary. The inner leads 131 have a thickness of 40 μ m whereas the portions of the lead frame 130 other than the inner leads 131 have a thickness of 0.15 mm which corresponds to the thickness of the lead frame blank. The other portions of the lead frame 130 except the inner leads 131 may not have the thickness of 0.15 mm, but have a thickness of 0.125 mm-0.50 mm which is thinner. The tips of the inner leads 131 have a small pitch of 0.12 mm so as to achieve an increase in the number of terminals for semiconductor devices. The second face 131Ab of the inner lead 131 has a substantially flat profile so as to allow an easy wire bonding thereon. Also, as shown in FIG. 1(b), because the third and fourth faces 131Ac and 131Ad have a concave shape which is depressed toward the inside of the associated inner lead, a high strength can be obtained even though the second face (wire bonding surface) 131Ab is narrowed.

In the present embodiment, since twisting does not

occur in the inner leads 131 irrespective of whether the
inner leads 131 is long or not. The inner leads having the
contour, as shown in FIG. 9(a), in which the tips of the
inner leads 131 are separated one from another, are
5 prepared by the etching process, and the inner leads are
resin-encapsulated after mounting the semiconductor chip
thereon as will be described later. However, where the
inner leads 131 are long in their length and have a
tendency for the generation of twisting therein, it is
10 impossible to fabricate the lead frame by etching to have
the contour as shown in FIG. 9(a). Therefore, after
etching the lead frame in a state where the tips of the
inner leads are fixed to the connecting portion 131B as
shown in FIG. 9(c)(1), the inner leads 131 are fixed with
15 the reinforcing tape 160 as shown in FIG. 9(c)(D). Then,
the connecting portions 131B which are not necessary in the
fabrication of the resin-encapsulated semiconductor device
are removed by a press as shown in FIG. 9(c)(A), and a
semiconductor device is then mounted on the lead frame.

20 Hereinafter, a method for the fabrication of the
resin-encapsulated semiconductor device will now be
described with reference to FIG. 8. First, the lead frame
130A, as shown in FIG. 9(a), which is shaped by the etching
process as will be described later, is prepared such that
25 the second surfaces 131Ab of the inner leads 131 are

directed upward (FIG. 8(a)).

Then, the semiconductor chip 110 is mounted onto the die pad 135 such that the surfaces of the semiconductor chip 110 on which the electrodes 111 are arranged, are
5 directed upward (FIG. 8(b)).

Next, after the semiconductor chip 110 is fastened onto the die pad 135, the electrodes 111 of the semiconductor chip 110 and the second surfaces 131ab of the inner leads 131 are bonded with each other using wires 120
10 (FIG. 8(c)).

Subsequently, encapsulation is carried out with the conventional resin encapsulate 140. Thereafter, unnecessary portions of the lead frame 130 which are protruded from the resin encapsulate 140 are cut by a press
15 to form terminal columns 133 and also the side surfaces 133b of the terminal columns 133 (FIG. 8(d)).

Then, the dam bars 136, the frame portions 137, etc. of the lead frame 130A as shown in FIG. 9 are removed. Next, the terminal portions 133A each made of the semi-
20 spherical solder are arranged on the outer surface of each terminal column 133 to fabricate a resin-encapsulated semiconductor device (FIG. 8(e)).

Thereafter, the protective frame 180 is arranged by means of adhesive around an entire outer surface of the
25 resultant structure in such a manner that the side surfaces

of the terminal columns 133 are covered thereby FIG.
6(f)). At this time, the protective frame 180 functions to
reinforce the semiconductor device. In other words, the
protective frame 180 serves to prevent moisture from
5 leaking into a gap between the resin encapsulate and the
terminal columns due to the fact that the side surfaces of
the terminal columns are exposed to the outside, whereby a
crack is not formed in the semiconductor device and the
breakage of the semiconductor device is avoided. However,
10 persons skilled in the art will readily appreciate that it
is not necessarily required to provide the protective frame
180. Also, when such an encapsulating process by the resin
is carried out using a desired mold, the encapsulating
process is implemented in a state wherein the outer side
15 surfaces of the terminal columns of the lead frame are
somewhat protruded out of the resin encapsulate.

A method for etching the lead frame of the first
embodiment will now be described in conjunction with the
attached drawings. FIG. 11 is of cross-sectional views
20 respectively illustrating sequential steps of the etching
process for the lead frame of the first embodiment. In
particular, the cross-sectional views of FIG. 1 correspond
to a cross section taken along the line D1-D2 of FIG. 9(a).
In FIG. 11, the reference numeral 1110 denotes a lead frame
25 blank, 1120A and 1120B resist patterns, 1130 first opening,

1140 second openings, 1150 first concave portions, 1160 second concave portions, 1170 flat surfaces, and 1180 an etch-resistant layer. First, a water-soluble casein resist using potassium dichromate as a sensitive agent is coated
5 over both surfaces of the lead frame blank 1110 made of a 42% nickel-iron alloy and having a thickness of about 0.15 mm. Using desired pattern plates, the resist films are patterned to form resist patterns 1120A and 1120B having first opening 1130 and second openings 1140, respectively
10 (FIG. 11(a)).

The first opening 1130 is adapted to etch the lead frame blank 1110 to have a flat etched bottom surface to a thickness smaller than that of the lead frame blank 1110 in a subsequent process. The second openings 1140 are adapted
15 to form desired shapes of tips of inner leads. Although the first opening 1130 includes at least an area forming the tips of the inner leads 1110, a topology generated by partially thinned portion by etching in a subsequent process can cause hindrance in a taping process or a
20 clamping process for fixing the lead frame. Thus, an area to be etched needs to be large without being limited to fine portions of the tips of the inner leads. Thereafter, both surfaces of the lead frame blank 1110 formed with the resist patterns are etched using a 48 Be' ferric chloride
25 solution of a temperature of 57°C at a spray pressure of

2.5 kg/cm². The etching process is terminated at the point of time when first recesses 1150 etched to have a flat etched bottom surface have a depth h corresponding to $1/3$ of the thickness of the lead frame blank (FIG. 11a).

5 Although both surfaces of the lead frame blank 1110 are simultaneously etched in the primary etching process, it is not necessary to simultaneously etch both surfaces of the lead frame blank 1110. The reason why both surfaces of the lead frame blank 1110 are simultaneously etched, as in
10 this embodiment, is to reduce the etching time taken in a secondary etching process as will be described later. The total time taken for the primary and secondary etching processes is less than that taken in the case of etching of only one surface of the lead frame blank on which the
15 resist pattern 1120B is formed. Subsequently, the surface provided with the first recesses 1150 respectively etched at the first opening 1130 is entirely coated with an etch-resistant hot-melt wax (acidic wax type MR-WB6, The Inctec Inc.) by a die coater to form an etch-resistant
20 layer 1180 so as to fill up the first recesses 1150 and to cover the resist pattern 1120A (FIG. 11(c)).

It is not necessary to coat the etch-resistant layer 1180 over the entire portion of the surface provided with the resist pattern 1120A. However, it is preferred that
25 the etch-resistant layer 1180 be coated over the entire

portion of the surface formed with the first recesses
and first opening 1130, as shown in FIG. 11(c), because
it is difficult to coat the etch-resistant layer 1180 on
the surface portion including the first recesses.
5 Although the etch-resistant layer 1180 wax employed in
this embodiment is an alkali-soluble wax, any suitable
wax resistant to the etching action of the etchant solution
remaining somewhat soft during etching may be used.
for forming the etch-resistant layer 1180 is not limited
10 to the above-mentioned wax, but may be a wax of a UV-cure
type. Since each first recess 1150 etched by the primary
etching process at the surface formed with the pattern
is adapted to form a desired shape of the inner lead track,
filled up with the etch-resistant layer 1180, it is
15 further etched in the following secondary etching process.
The etch-resistant layer 1180 also enhances the mechanical
strength of the lead frame blank for the second etching
process, thereby enabling the second etching process to be
conducted while keeping a high accuracy. It is
20 possible to enable a second etchant solution to be sprayed
at an increased spraying pressure, for example, 2.5 kg/cm²
or above, in the secondary etching process. The increased
spraying pressure promotes the progress of etching in the
direction of the thickness of the lead frame blank in the
25 secondary etching process. Then, the lead frame blank

surfaces 131Aa of the tips of the inner leads as shown in
FIG. 1, are flushed with one surfaces of remaining portions
of the inner leads having the same thickness with the lead
frame while being opposed to the second surfaces 131Ab, and
the third and fourth surfaces are formed to have a concave
shape which is depressed toward the inside of the inner
leads. Where a semiconductor chip is mounted on the second
surfaces 131Ab of the inner leads by means of bumps for an
electrical connection therebetween, as in a semiconductor
device according to a third embodiment as will be described
hereinafter, an increased tolerance for the connection by
bumps is obtained when the second surface 131Ab has a
concave shape depressed toward the inside of the inner
lead. To this end, an etching method shown in FIG. 12 is
adopted in this case. The etching method shown in FIG. 12
is the same as that of FIG. 11 in association with its
primary etching process. After completion of the primary
etching process, the etching method is conducted in a
manner different from that of the etching method of FIG. 11
in that the second etching process is conducted at the side
of the first recesses 1150 after filling up the second
recesses 1160 by the etch-resist layer 1180, thereby
completely perforating the second recesses 1160. At this
time, by implementing the primary etching process, etching
at the side of the second openings 1140 is performed in a

sufficient manner. The cross section of each inner lead, including its tip, formed in accordance with the etching method of FIG. 12, has a concave shape depressed toward the inside of the inner lead at the second surface 131Ab, as shown in FIG. 6(b).

The etching method in which the etching process is conducted at two separate steps, respectively, as in that of FIGs. 11 and 12, is generally called a "two-step etching method". This etching method is advantageous in that a desired fineness can be obtained. The etching method used to fabricate the lead frame 130A of the first embodiment shown in FIG. 9 involves the two-step etching method and the method for forming a desired shape of each lead frame portion while reducing the thickness of each pattern formed. In particular, the etching method makes it possible to achieve a desired fineness. In accordance with the method illustrated in FIGs. 11 and 12, the fineness of the tip of each inner lead 131A formed by this method is dependent on the shape of the second recesses 1160 and the thickness t of the inner lead tip which is finally obtained. For example, where the blank has a thickness t reduced to 50 μ m, the inner leads can have a fineness corresponding to a lead width W_1 of 100 μ m and a tip pitch p of 0.15 mm, as shown in FIG. 11(e). In the case of using a small blank thickness t of about 30 μ m and a lead

width W_1 of 70 μm , it is possible to form inner leads having a fineness corresponding to an inner lead pitch p of 0.12 μm . Of course, it may be possible to form inner leads having a further reduced tip pitch by adjusting the blank thickness t and the lead width W_1 . That is to say, an inner lead tip pitch p up to 0.08 μm , a blank thickness up to 25 μm , and a lead width W_1 up to 40 μm can be obtained.

In the case where twisting of the inner leads does not occur in the fabricating process, as in the case where the inner leads are short in their length, a lead frame illustrated in FIG. 9(a) can be directly obtained. However, where the inner leads are long in length as compared to those of the first embodiment, the inner leads have tendency for the generation of twisting. Thus, in this case, the lead frame is obtained by etching in a state where the tips of the inner leads are bound to each other by a connecting member 131B as shown in FIG. 9(c)(1). Then, the connecting member 131B which is not necessary for the fabrication of a semiconductor package is cut off by means of a press to obtain a lead frame shaped as shown in FIG. 9(a).

Moreover, as described above, where unnecessary portions in a structure shown in FIG. 9(c)(1) are cut to obtain the lead frame having the contour shown in FIG.

9(a), a reinforcing tape 160 is a polyimide tape is generally used, as shown in FIG. 9(c)(A). While the connecting member 131B is cut off by means of a press to obtain the contour shown in FIG. 9(c)(D), a semiconductor device is mounted on the lead frame still having the reinforcing tape attached thereon. Also, the mounted semiconductor device is encapsulated with a resin in a condition where the lead frame still has the tape. The line E11-E12 illustrates a cut portion.

The tip of the inner lead 131 of the lead frame used in the semiconductor device of this first embodiment has a cross-sectional shape as shown in FIG. 13(1)(a). The tip 131A has an etched flat surface (second surface) 131Ab which is substantially flat and therefore has a width W1 slightly greater than the width W2 of an opposite surface. The widths W1 and W2 (about 1000 μ m) are more than the width W at the central portion of the tips when viewed in the direction of the inner lead thickness. Thus, the tip of the inner lead has a cross-sectional shape having opposite wide surfaces. To this end, although either of the opposite surfaces of the tip 131A can be easily electrically connected to a semiconductor device (not shown) by a wire 120A or 120B, this embodiment illustrates the use of the etched flat surface for wire-bonding as shown in FIG. 13(D)(a). In FIG. 13, a reference numeral

131Ab depicts an etched flat surface, 131Aa a surface of a lead frame blank, and 121A and 121B, respectively, a plated portion. In the case of FIG. 13(D)(a), there has particularly excellent in wire-bonding property, because the etched flat surface does not have roughness. FIG. 13(A) shows that the tip 1331B of the inner lead of the lead frame fabricated according to the process illustrated in FIG. 14 is wire-bonded to a semiconductor device. In this case, however, both the opposite surfaces of the tip 1331B of the inner lead are flat, but have a width smaller than that in a direction of the inner lead thickness. In addition to this, as both the opposite surfaces of the tip 1331B is formed of surfaces of the lead frame blank, these surfaces have an inferior wire-bonding property as compared to that of the etched flat surface of this first embodiment. FIG. 13(B) shows that the inner lead tip 1331C or 1331D, obtained by thinning in its thickness by a means of a press (coining) and then by etching, is wire-bonded to a semiconductor device (not shown). In this case, however, a pressed surface of the inner lead tip is not flat as shown FIG. 13(B). Thus, the wire-bonding on either of the opposite surfaces as shown in FIG. 13(B)(a) or FIG. 13(B)(b) often results in an insufficient wire-bonding stability and a problematic quality. The drawing reference numeral 1331Ab represents a coining surface.

A modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention will be described hereinafter. FIGs. 3(a) through 3(e) are cross-sectional views of the modified example of the resin-encapsulated semiconductor device in accordance with the first embodiment of the present invention. The semiconductor device of the modified example as shown in FIG. 3(a), is different from that of the first embodiment in that a position of the die pad 135 is changed, that is, the die pad 135 is exposed to the outside. By the fact that the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Also, in the semiconductor device of the modified example as shown in FIG. 3(b), because the die pad 135 is exposed to the outside, the heat dissipation property is improved as compared to the first embodiment. Unlike the first embodiment or the modified example as shown in FIG. 3(a), in the present modified example as shown in FIG. 3(b), because a direction of the semiconductor device 110 is changed, the first surfaces of the lead frame are established as the wire bonding surfaces. The modified examples as shown in FIGs. 3(c), 3(d) and 3(e), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the first embodiment, the modified

example as shown in FIG. 3(a) and the modified example as shown in FIG. 3(b), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions, whereby an entire manufacturing procedure can be simplified.

Next, a resin-encapsulated semiconductor device in accordance with a second embodiment of the present invention will be described. FIG. 4(a) is a cross-sectional view of the resin-encapsulated semiconductor device in accordance with the second embodiment of the present invention, FIG. 4(b) is a cross-sectional view illustrating inner leads, taken along the line A3-A4 of FIG. 4(a), and FIG. 4(c) is a cross-sectional view illustrating a terminal column, taken along the line B3-B4 of FIG. 4(a). Because an outer appearance of the semiconductor device of the second embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 3, the drawing reference numeral 200 represents a semiconductor device, 210 a semiconductor chip, 211 electrodes (pads), 220 wires, 230 a lead frame, 231 inner leads, 231Ab a second surface, 231Ac a third surface, 231Ad a fourth surface, 233 terminal columns, 233A terminal portions, 233B side surfaces, 233S top surfaces, 240 a resin encapsulate, and 270 a reinforcing fastener tape. In the semiconductor device of

this second embodiment, the lead frame 230 does not have a die pad, the semiconductor chip 210 is fastened to the inner leads 231 by the reinforcing fastener tape 270, and the semiconductor chip 210 is electrically connected at its electrodes (pads) 211 to the second surfaces 231Ab of the inner leads 231 by wires 220. Also, in the case of this second embodiment, similarly to the first embodiment, the electrical connection between the resin-encapsulated semiconductor device 200 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 200 via the terminal portions 233A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 233A located on the top surfaces 233S of the terminal columns 233, respectively.

In addition, the semiconductor device of this second embodiment does not have a die pad as shown in FIGs. 10(a) and 10(b). The manufacturing method of the semiconductor device of this embodiment using the lead frame 230A which is shaped by the etching process is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of the second embodiment, the wire

bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 210 is fastened together with the inner leads 231 by the reinforcing fastener tape 270. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment. The lead frame 230 as shown in FIG. 10(a) is obtained in the same manner by which the lead frame 130A as shown in FIG. 9(a) is obtained. In other words, by cutting the resultant structure obtained after etching the structure as shown in FIG. 10(c)(1), the contour as shown in FIG. 10(a) is obtained. At this time, the conventional reinforcing fastener tape 260 (the polyimide tape) as shown in FIG. 10(c)(2), which performs a reinforcing function is used.

FIG. 5(a) through 5(c) are cross-sectional views illustrating modified examples of the semiconductor device of the second embodiment. The semiconductor device as shown in FIG. 5(a) is different from the semiconductor device of the second embodiment, in that the surface of the semiconductor chip thereof which has the electrodes is directed downward. The modified examples as shown in FIGs. 5(b) and 5(c), illustrate semiconductor devices which are obtained by modifying the semiconductor devices of the second embodiment and the modified example as shown in FIG.

5(a), wherein the semi-spherical solders are not used, and instead, the top surfaces of the terminal columns are directly used as the terminal portions. In these examples, because a protective frame is not used and the side surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

Hereinafter, a resin-encapsulated semiconductor device in accordance with a third embodiment of the present invention will be described. FIG. 6(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the third embodiment, FIG. 6(b) is a cross-sectional view illustrating inner leads, taken along the line A5-A6 of FIG. 6(a), and FIG. 6(c) is a cross-sectional view illustrating a terminal column, taken along the line B5-B6 of FIG. 6(b). Because an outer appearance of the semiconductor device of the this third embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 6, the drawing reference numeral 300 represents a semiconductor device, 310 a semiconductor chip, 312 bumps, 330 a lead frame, 331 inner leads, 331Aa a first surface, 331Ab a second surface, 331Ac a third surface, 331Ad a fourth surface, 333 terminal columns, 333A terminal portions, 333B side surfaces, 333S top surfaces, 340 a resin encapsulate, and 350 a

reinforcing fastener tape. In the semiconductor device of this third embodiment, the semiconductor chip 310 is fastened to the second surfaces 331Ab of the inner leads 331 by the bumps 311 thereby to be electrically connected to the second surfaces 331Ab. The lead frame 330 has a contour as shown in FIGs. 10(a) and 10(b), which is formed by the etching process of FIG. 11. As shown in FIG. 13(1)(b), both widths W1A and W2A (about 100 μ m) at top and bottom ends of the inner leads 331 are larger than a width WA at a center portion in a thickness-wise direction. Due to the fact that the second surfaces 331Ab of the inner leads 331 is depressed toward the inside of the inner leads and the first surfaces 331Aa are flat, a desired fineness can be obtained. Also, when the second surfaces 331Ab of the inner leads 331 are electrically connected to the semiconductor chip via bumps, easy connection can be accomplished as shown in FIG. 13(D)(b). Further, in the case of this third embodiment, as in the case of the first and second embodiments, the electrical connection between the resin-encapsulated semiconductor device 300 of this embodiment and an external circuit is achieved by mounting the resin-encapsulated semiconductor device 300 via the terminal portions 333A each being made of a semi-spherical solder, on a printed circuit substrate, with the terminal portions 333A located on the top surfaces of the terminal

columns 333, respectively.

In addition, unlike the semiconductor device of the first embodiment, the semiconductor device of this third embodiment uses a lead frame which is shaped by the etching process as shown in FIG. 12. However, the manufacturing method of the semiconductor device of this embodiment is substantially the same as that of the first embodiment except that, while in the case of the first embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip is fastened to the inner leads, in the case of this third embodiment, the wire bonding process and resin encapsulating process are performed in a state wherein the semiconductor chip 310 is fastened to the inner leads 331 via the bumps. Also, the cutting process for the unnecessary portions and the terminal portion forming process after resin encapsulating process are implemented in the same way as the first embodiment.

FIG. 6(d) is a cross-sectional view illustrating a modified example of the semiconductor device in accordance with the third embodiment of the present invention. In the modified example of the semiconductor device as shown in FIG. 6(d), the terminal portions each comprising the semi-spherical solder are not provided, and the top surfaces of the terminal columns are directly used as the terminal

portions. Because the protective frame is not used and the side surfaces 333B of the terminal columns 333 are exposed to the outside, a checking operation by a test, etc. can be easily performed.

5 Hereinafter, a resin-encapsulated semiconductor device in accordance with a fourth embodiment of the present invention will be described. FIG. 7(a) is a cross-sectional view of the resin-encapsulated semiconductor device of the fourth embodiment, FIG. 7(b) is a cross-sectional view illustrating inner leads, taken along the line A7-A8 of FIG. 7(a), and FIG. 7(c) is a cross-sectional view illustrating a terminal column, taken along the line 37-38 of FIG. 7(b). Because an outer appearance of the semiconductor device of the this fourth embodiment is substantially the same as that of the first embodiment, it is not illustrated in the drawings. In FIG. 7, the drawing reference numeral 400 represents a semiconductor device, 10 410 a semiconductor chip, 411 pads, 430 a lead frame, 431 inner leads, 431Aa a first surface, 431Ab a second surface, 431Ac a third surface, 431Ad a fourth surface, 433 terminal columns, 433A terminal portions, 433B side surfaces, 433S top surfaces, 440 a resin encapsulate, and 470 insulating adhesive. In the semiconductor device of this fourth embodiment, one surface of the semiconductor chip 410 on 20 which the pads 411 are disposed is fastened to the second 25

surfaces 431Ab of the inner leads 431 by the insul-
adhesive 470, and the pads 411 and the first surfaces
of the inner leads 431 are electrically connected with
other by wires 420. The semiconductor device of
5 fourth embodiment uses the same lead frame which is use
the third embodiment, which has the contour as shown
FIG. 10(a) and 10(b). Also, in the case of this fourth
embodiment, as in the case of the first and second
embodiments, the electrical connection between the res-
10 encapsulated semiconductor device 400 of this embodiment
and an external circuit is achieved by mounting the res-
encapsulated semiconductor device 400 via the terminal
portions 433A each being made of a semi-spherical solder
on a printed circuit substrate, with the terminal portion
15 433A located on the top surfaces of the terminal columns
433, respectively.

FIG. 7(d) is a cross-sectional view illustrating
modified example of the semiconductor device in accordance
with the fourth embodiment of the present invention. In
20 the modified example of the semiconductor device as shown
in FIG. 7(d), the terminal portions each comprising the
semi-spherical solder are not provided, and the top
surfaces of the terminal columns are directly used as the
terminal portions. Because the protective frame is not
25 used and the side surfaces 433B of the terminal columns 433

are exposed to the outside, a checking operation by a test, etc. can be easily performed.

(EFFECTS OF THE INVENTION)

5 The present invention provides a resin-encapsulated semiconductor device employing the above-mentioned lead frame, which is capable of meeting a demand for the increased terminal number. Furthermore, the resin-encapsulated semiconductor device in accordance with this invention does not require a process of cutting or bending the dam bars as in the case of using a lead frame having 10 outer leads as shown in FIG. 13(b). As a result of this, the resin-encapsulated semiconductor device does not have a problem in that the outer leads are bent, or a problem associated with coplanarity. In addition to these 15 advantages, the resin-encapsulated semiconductor device has a shortened interconnection length as compared to the QTP or the BGA, whereby the semiconductor device can be reduced in a parasitic capacity, and shortened in a transfer delay 20 time.

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